1. (previously presented) A power supply controller which directs the supply of a plurality of different voltages from a power supply unit, comprising:

a state register circuit to store state values corresponding to a combination of voltages supplied by the power supply unit;

a reference clock oscillator circuit;

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit;

a state value changing combination circuit which changes the state values one by one in a predetermined order corresponding to a target combination of voltages when the change instruction is received to change the combination of voltages supplied by the power supply unit;

an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by said state value changing combination circuit to the power supply unit, wherein an information processor to which the plurality of voltages are supplied has a plurality of sections operating on the plurality of voltages;

said state register circuit has state values of combinations of voltages respectively supplied to the plurality of sections;

when said state value changing combination circuit receives the change instruction to change the combination of voltages supplied to the plurality of sections it changes the state values in a predetermined order indicating for which one of the sections the voltage should be changed first;

said output section supplies the combinations of voltages corresponding to the state values changed one by one from the power supply unit to the sections of the information processor;

wherein a predetermined combination of voltages provided to the sections of the information processor are supplied through one of a plurality of operating modes discriminated in power consumption in the information processor; and

when the state value changing combination circuit receives an invalid change instruction corresponding to none of the plurality of operating modes, it sets the state values for supplying a combination of voltages representing the nearest corresponding valid operating mode.

2. (original) The power supply controller according to Claim 1, wherein the change instruction specifying a power on sequence of the combination of supplied voltages starts with the lowest supplied voltage.

3. (original) The power supply controller according to Claim 1, wherein the change instruction specifying a power off sequence of the combination of supplied voltages, starts from the highest supplied voltage.

4. (canceled).

5. (previously presented) The power supply controller according to Claim 1, wherein said reference clock is enabled after receiving the change instruction to supply a voltage to one of the plurality of sections of the information processor.

6. (previously presented) The power supply controller according to Claim 1, wherein said reference clock is disabled after receiving the change instruction to stop supplying voltages to all the sections of the information

processor and said state value changing combination circuit has stopped supplying the plurality of voltages to all the sections.

7. (previously presented) The power supply controller according to Claim 1, wherein said reference clock oscillator circuit further comprises:

a delay circuit to provide a delayed change instruction signal;

a first logic gate that determines the logical sum of the delayed change instruction signal and the undelayed change instruction signal;

an RC delay circuit to provide a delayed reference clock signal; and

a Schmidt inverter which accepts the output from the RC delay circuit; and

a second logic gate that determines the logical product of the output of the Schmidt inverter and the output of the first logic gate and completes a feedback loop for the reference clock.

8. (canceled).

9. (currently amended) A power supply controller which controls a power supply unit having a plurality of power supplies each of which can be independently set to a plurality of states, said power supply controller comprising:

a state register circuit to store state values corresponding to a combination of voltages supplied by the power supply unit;

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit;

a state value changing combination circuit which changes the state values one by one in a predetermined order corresponding to the temporal order in which a target combination of voltages is desired to be received when the change instruction is received to change the combination of voltages supplied by the power supply unit; and

an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by the state value changing combination circuit to the power supply unit.

10. (currently amended) An information processor which operates using a plurality of different operating voltages comprising:

a state register section which stores state values corresponding to a combination of voltages supplied to the information processor;

a reference clock oscillator circuit;

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied to the information processor;

a state value changing combination circuit which changes the state values one by one in a predetermined order corresponding to the temporal order in which a target combination of voltages is desired to be received when the change instruction is received to change the combination of voltages supplied by the power supply unit;

an output section through which the information processor is supplied the combination of voltages corresponding to the state values successively changed by said state value changing combination circuit; and

a power supply unit which supplies power to the information processor according to an instruction from said output section.

11. (original) The information processor according to Claim 10, further comprising a plurality of sections operating on the plurality of voltages,

wherein said state register section stores combinations of voltages respectively supplied to the plurality of sections;

said state value changing combination circuit changes the state values in a predetermined order indicating for which one of the sections the voltage should be changed first; and

said output section supplies the combinations of voltages corresponding to the state values changed one by one from the power supply unit to the sections of the information processor.

12. (original) The information processor according to Claim 11, wherein said reference clock is enabled when the change instruction to supply a voltage to one of the plurality of sections is received.

13. (original) The information processor according to Claim 11, wherein said reference clock is disabled when the change instruction to stop supplying voltages to all the sections of the information processor is received

and said state value changing combination circuit has stopped supplying the plurality of voltages to all the sections.

14. (currently amended) An information processor which operates using a plurality of power supplies each of which can be independently set in an on or off state, said information processor comprising:

a state register section which stores state values corresponding to a combination of voltages supplied to the information processor;

a reference clock oscillator circuit;

a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied to the information processor;

a state value changing combination circuit which changes the state values one by one in a predetermined order corresponding to the temporal order in which a target combination of voltages is desired to be received when the change instruction is received to change the combination of voltages supplied by the power supply unit;

an output section through which the information processor is supplied the combination of voltages corresponding to the state values successively changed by said state value changing combination circuit; and

a power supply unit which supplies power to the information processor according to an instruction from said output section.

15. (previously presented) A method of supplying a plurality of voltages from a multiple voltage level power supply to an information processor, the method comprising:

providing a state register circuit to store state values corresponding to a combination of voltages supplied by the power supply unit;

providing a reference clock oscillator circuit;

providing a state value setting combination circuit which generates a change instruction to change the combination of voltages supplied by the power supply unit;

providing a state value changing combination circuit which changes the state values one by one in a predetermined order corresponding to a target combination of voltages when the change instruction is received to change the combination of voltages supplied by the power supply unit; and

providing an output section to transmit the combination of voltages corresponding to the change instruction state values successively changed by said state value changing combination circuit to the power supply unit;

providing a delay circuit within the reference clock oscillator circuit to delay a change instruction signal input to the reference clock oscillator circuit;

providing a first logic gate that determines the logical sum of the delayed change instruction signal and the undelayed change instruction signal;

providing an RC delay circuit to provide a delayed reference clock signal;

providing a Schmidt inverter which inputs the RC delay circuit output; and

providing a second logic gate that determines the logical product of the output of the Schmidt inverter and the output of the first logic gate and completes a feedback loop for the reference clock.

16. (previously presented) The method according to Claim 15 further comprising:

structuring the change instruction such that a power on sequence of the combination of supplied voltages begins with the lowest supplied voltage; and

structuring the change instruction such that a power off sequence of the combination of supplied voltages begins with the highest supplied voltage.

17. (previously presented) The method according to Claim 15 further comprising:

storing said combinations of voltages respectively supplied to the plurality of sections in the state register circuit;

programming said state value changing combination circuit such that the state values are changed in a predetermined order indicating for which one of the sections the voltage should be changed first; and

supplying said combinations of voltages corresponding to the state values changed one by one from the power supply unit to the sections of the information processor.

18. (previously presented) The method according to Claim 15 further comprising:

enabling said reference clock after receiving the change instruction to supply a voltage to one of the plurality of sections of the information processor.

19. (previously presented) The method according to Claim 15 further comprising:

disabling said reference clock after receiving the change instruction to stop supplying voltages to all the sections of the information processor and said state value changing combination circuit has stopped supplying the plurality of voltages to all the sections.

20 (canceled).